REMARKS

Claims 1-68 and 82-94 are cancelled; and claims 69-81 remain pending in the application.

The undersigned conducted a telephone interview with the Examiner on April 5, 2005, to discuss the rejections currently pending against the claims. The undersigned thanks the Examiner for the courteousness and helpfulness extended during such interview, and has provided an Interview Summary accompanying this Response.

The independent claims pending in the application (claims 69 and 81) recite constructions containing PMOS gates and NMOS gates which each comprise n-type doped silicon over metal-containing materials, with the metal-containing material of the PMOS gate being thicker than that of the NMOS gate. Specifically, the claims recite that the PMOS gate has metal-containing material with a thickness of greater than 20Å, while the NMOS gate has metal-containing material with a thickness of less than or equal to about 20Å. The references cited against the claims of the application are Tonti (U.S. Patent No. 6,436,749 and Chau (U.S. Publication No. 2003/0129793).

Applicant believes that the pending claims are allowable over the cited combination of Tonti and Chau for at least the reason that there is no teaching amongst the references for the recited structures having the PMOS gate with a thicker metal-containing material than the NMOS gate.

The Examiner cites Chau for disclosing that metal-containing material utilized within gates can be formed within a range of thicknesses which can include thicknesses below 20Å and thicknesses above 20Å. However, as discussed during the telephone interview, there is no teaching within Chau which suggests that the metal-containing material utilized in an NMOS gate would be of a different thickness than that utilized in the PMOS gate. Rather, the considerations expressed in Chau for determining the thickness of a metal-containing layer to be utilized in various gates would apply equally to NMOS gates and PMOS gates, and would thus seem to suggest that the same thickness of metal-containing material is utilized in both NMOS gates and PMOS gates, or at least doesn't suggest the recited structures of claims 69 and 81 of metal-containing materials utilized in the recited PMOS gates that are thicker than metal-containing materials utilized in the recited NMOS gates. The cited reference of Tonti describes CMOS constructions, and indicates that n-type semiconductive material can be utilized in both PMOS gates and NMOS gates. However, Tonti, like Chau, doesn't disclose or suggest that a metal-containing material utilized in an NMOS gate would be of a different thickness than the metal-containing material utilized in a PMOS gate, and accordingly the combination of Chau and Tonti doesn't contain any suggestion or disclosure that metal-containing material utilized in an NMOS gate would be of a different thickness than the metal-containing material utilized in a PMOS gate.

For the above-discussed reasons, claims 69-81 are believed allowable over the cited combination of Tonti and Chau, and Applicant therefore respectfully requests such allowance in the Examiner's next action.

Respectfully submitted,

Dated: April 7, 2005 By: _____
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Enclosure: Interview Summary